REMARKS

Claims 1-3 and 7-22 are pending in the instant application. Claims 2-3 and 7-22 are amended herein. No new matter has been added as a result of the amendments.

PRIORITY

The rejection has purported that the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 1-22 of the present application. Applicants respectfully disagree. Support for the claimed embodiments of the present invention is shown in at least the following locations of the provisional application.

The Applicants direct the Examiner to the Claims section of the provisional application entitled "WE CLAIM." Claim 1 of the provisional recites (emphasis added):

> a microprocessor;
> a plurality of programmable analog circuit blocks; and
> a plurality of programmable digital circuit blocks, at least one of said programmable circuit blocks being coupled directly or indirectly to at least one of said programmable analog circuit blocks;
> wherein at least a first one of said programmable digital circuit blocks is coupled directly or indirectly to at least a first one of said programmable analog circuit blocks, and at least a second of said programmable digital circuit blocks and said programmable analog circuit blocks is coupled directly or indirectly to said microprocessor.

Claim 9 of the provisional application recites in part (emphasis added):

> The circuit of Claim 1 further comprising a plurality of input and or output blocks, coupled directly or indirectly to at least one of said programmable memory, said programmable digital circuit blocks, said plurality of programmable analog circuit blocks, and said microprocessor.

Claims 1 and 9 of the provisional application provide support for the claimed

limitations of the present invention including support for at least the microprocessor, a digital circuit, an analog circuit and a plurality of input and output pins.

Further support for the input and output pins is provided in the provisional application on at least the page entitled "PSoC Technology Background Information."

Further support for a switching circuit that selectively connects at least one of the analog input, analog output, digital input, and digital output is provided in the provisional application on the page entitled "IO Pins." Further support for this feature is in the provisional application on the page entitled "Fixed Function SoCblocs," specifically, "Digital IO Pin Global Routing."

Further support for the claimed embodiments of the present invention is included in the provisional application on the page entitled "Global IO Routing," specifically:

> every IO pin can be routed on-to or off-of a set of 16 global digital signal lines. This allows pin assignments to internal functions to be set by the customer during configuration or during firmware execution. Global routing is parameterized within each IO pin yielding flexibility in pin-out choice.

A supporting schematic of the claimed limitations of the present invention is provided in the provisional application on the page entitled, "Hardware Routing Resources."

Support for a processor comprising an analog circuit, a digital circuit and programmable pin configurations is provided on the page entitled "Cypress MicroSystems CY8C25xxx/26xxx Data Sheet of the provisional application." Further

support for the programmable interconnects is provided on the page entitled Cypress MicroSystems CY8C25xxx/26xxx Data Sheet 1.3 Block Diagram."

For this rational, Applicants assert that the provisional application provides ample support for the claimed limitations of the instant application. As such, Applicants request that the instant application be granted the priority date of the provisional application, which is October 26, 2000.

DRAWINGS

The drawings are objected to in the outstanding Office Action. The specification has been amended herein in a manner so as to obviate the objection to the drawings. Consequently, the Applicants respectfully request the withdrawal of the drawing objections made in the outstanding Office Action.

Claim Objections

The Examiner objected to the Claims as containing informalities. The Claims have been amended herein so as to eliminate any informalities. Consequently, the Applicants respectfully request the withdrawal of the objections to the Claims.

112 Rejections

The claims have been amended herein to obviate the rejection of Claims 1-22 under 35 U.S.C. 112. Therefore, the Applicants respectfully request the withdrawal of the rejection of Claims 1-22 under 35 U.S.C. 112.

102 Rejection

Claims 1 and 3 are rejected under 35 U.S.C 102(e) as being anticipated by U.S. Patent No. 6,356,958 to Lin, hereafter referred to as Lin. The rejection is respectfully traversed for the following rational.

The Examiner is respectfully directed to independent Claim 1 which sets forth an embodiment of the present invention including:

> ... a circuit comprising an analog circuit and a digital circuit wherein said analog circuit comprises an analog input and an analog output, and said digital circuit comprises a digital input and a digital output; a wirebond pad; a processor; and a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor.

Claim 3 depends from Claim 1 and recites further features of the claimed invention.

Lin does not teach or suggest a microcontroller that includes a switching circuit and a wirebond pad wherein "at least one of said analog input, said analog output, said digital input and said digital output" are selectively connected by the switching circuit to the wirebond pad as is recited in Claim 1. In fact, Lin teaches away from the claimed embodiment by teaching in the Abstract "The selectable functions are selected during packaging of the known good integrated circuit die."

This is very different from "a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor," as claimed. Lin purports to teach selecting the desired circuit functionality prior to packaging and the claimed invention selectively connects functionality at any time after packaging and is in fact, user configurable. Consequently, Lin fails to teach or suggest the embodiment of the Applicants' invention as set forth in Claim 1. As such, Claims 1 and 3 are not anticipated by Lin. As such, Claims 1 and 3 are patentable over Lin and are in condition for allowance. As such, Applicants respectfully solicit allowance of Claims 1 and 3 based on this rational.

103 Rejection

Claims 1, 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,509,758 to Piasecki et al., hereafter referred to as Piasecki in view of the reference, Wirebonding: Reinventing the process for MCMs by H.K. Charles, et al., hereafter referred to as Charles. Piasecki and the claimed invention are very different. Piasecki teaches in column 2 lines 24-27 "a pin interface which allows both analog and digital

signals to be coupled to respective processing circuits, via a single I/) pin." This is very different form the claimed embodiment. The claimed embodiment comprises "an analog input, an analog output, a digital input and a digital output."

The claimed embodiment uses dedicated pins for analog input and analog output and dedicated pins for digital input and digital output. Piasecki uses a single pin for both digital and analog input, which teaches away from the claimed embodiment.

Charles fails to remedy the deficiencies of Piasecki. Charles may purport to teach a wirebonding pad, however, Charles fails to teach or suggest "a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor," as claimed. As such, Claim 1 is patentable over Piasecki in view of Charles. Therefore, Claim 1 is in condition for allowance and allowance of Claim 1 is earnestly solicited for this rational.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,555,452 to Calloway, Jr., et al., hereafter referred to as Calloway in view of Charles. The rejection is respectfully traversed for the following rational.

Applicants have reviewed the Calloway reference and respectfully assert that Calloway fails to teach or suggest the claim limitations of the present invention. Calloway purports to teach a peak and valley measuring circuit. This is very different from "a switching circuit that selectively connects at least one of said analog input, said analog output, said

digital input and said digital output to the wirebond pad under control of the processor," as claimed.

In fact, Calloway teaches away from the claimed limitations of the present invention by teaching in column 3 lines 44-50, "the selecting circuitry 180 triggers the peak counter 110 to count at a current peak only when the current peak is greater than a prior peak and triggers the valley counter 120 to count at a current valley only when the current valley is less (larger in magnitude) than a prior valley." Calloway switches between a peak counter and a valley counter based on current. The switching of the present invention is between "at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor," as claimed.

Charles fails to remedy the deficiencies of Calloway. Charles may purport to teach a wirebond pad, however, Charles fails to teach or suggest "at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor," as claimed. For this rational, Claim 1 is patentable over Calloway in view of Charles. As such, Claim 1 is in condition and allowance of Claim 1 is earnestly solicited.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,305,312 to Fornek, et al., hereafter referred to as Fornek in view of Charles. The rejection is respectfully traversed for the following rational.

Fornek may purport to teach a voice data controller. However, Fornek and the claimed invention are very different. Claim 1 recites "a circuit comprising an analog circuit and

a digital circuit wherein said analog circuit comprises an analog input and an analog output and said digital circuit comprises a digital input and a digital output." This is very different from the teachings of Fornek.

In fact Fornek teaches away from the claimed limitations of the instant application because Fornek teaches the analog and digital interfaces are coupled to the processor via two different communication busses. For example, in column 5 lines 18-20, Fornek teaches "analog interfaces are also connected to ISDN bus 220 and are under the control of processor 225 via system bys 235 and ISDN bus 220." This is very different from "a circuit comprising an analog circuit and a digital circuit wherein said analog circuit comprises an analog input and an analog output and said digital circuit comprises a digital input and a digital output," as claimed. The claimed embodiment comprises a single circuit comprising a digital circuit with a corresponding digital input and a digital output, and an analog circuit with corresponding analog input and analog output.

Charles fails to remedy the deficiencies of Fornek. Charles may purport to teach a wirebond pad, however, Charles fails to teach or suggest "a circuit comprising an analog circuit and a digital circuit wherein said analog circuit comprises an analog input and an analog output and said digital circuit comprises a digital input and a digital output," as claimed. For this rational, Claim 1 is patentable over Fornek in view of Charles. As such, Claim 1 is in condition for allowance and allowance of Claim 1 is earnestly solicited.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of U.S. Patent No. 6,768,337 to Kohno, et al., hereafter referred to as Kohno. The rejection is traversed for the following rational.

For the rational stated above for Claim 1, Lin fails to teach or suggest "a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor," as claimed. Kohno fails to remedy the deficiencies of Lin. In fact, Kohno fails to teach or suggest "a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor," as claimed.

Furthermore, the Kohno reference has a priority date of August 21, 2001 which is subsequent the effective priority date of the instant application, October 26, 2000. For this rational, Claim 2 is patentable over Lin in view of Kohno. As such, Claim 2 is in condition for allowance and allowance of Claim 2 is earnestly solicited.

Claims 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of U.S. Patent No. 5,107,146 to El-Ayat, hereafter referred to as El-Ayat. The rejection is traversed for the following rational.

For the rational stated above for Claim 1, Lin fails to teach or suggest "a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor," as claimed. El-Ayat fails to remedy the deficiencies of Lin.

In fact, El-Ayat teaches away from the claimed embodiment by teaching in the abstract, "a user configurable interface for conversion of signals from analog to digital form

and from digital form to analog form." This is significantly different from "selectively connecting at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor," as claimed. For this rational, Claims 7-22 are patentable over Lin in view of El-Ayat. As such, Claims 7-22 are in condition for allowance and allowance of Claims 7-22 is earnestly solicited.

Conclusion

In light of the above-listed remarks, the Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact the Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Dated: 11/4, 2004

Anthony Murabito
Registration No. 35,295

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060